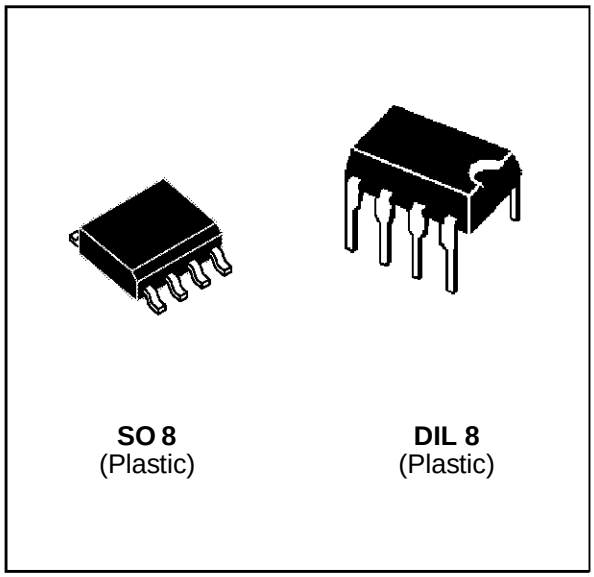
SGS-THOMSON MICROELECTRONICS

TPI80xxN/TPI120xxN

TRIBALANCED PROTECTION WITH LOW DYNAMIC V_{BO} FOR ISDN INTERFACES

FEATURES

- BIDIRECTIONAL TRIPLE PROTECTION.
- CROWBAR PROTECTION.
- PEAK PULSE CURRENT :
  I_{PP} = 30 A , 10/1000 µs.
- BREAKDOWN VOLTAGE:
  TPI80N = 80V
  TPI120N = 120V.
- AVAILABLE IN DIL8 AND SO8 PACKAGES.
- LOW DYNAMIC BREAKOVER VOLTAGE :
  TPI80N = 150V
  TPI120 = 200V



SO 8
(Plastic)

DIL 8
(Plastic)

DESCRIPTION: TRIBALANCED PROTECTION

Dedicated devices for ISDN interface and high speed data telecom lines protection. Equivalent to a triple TRISIL with low capacitance providing:

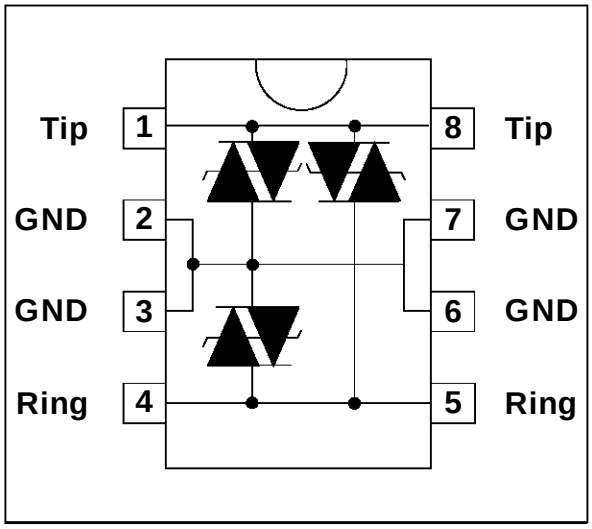
Low capacitance from lines to ground :
allowing high speed transmission without signal attenuation.

Good capacitance balance (Line A/Line B) in order to insure the longitudinal balance of the line.

Fixed breakdown voltage in both common and differential modes.

The same surge current capability in both common and differential modes.

SCHEMATIC DIAGRAM

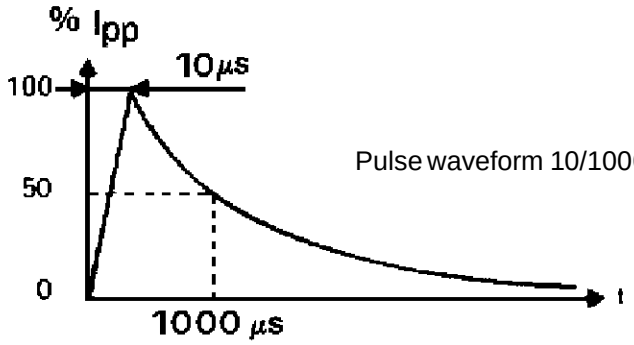


IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (-40°C ≤ Ta ≤ +85°C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 5/320 µs 2/10 µs	30 40 90	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 10 ms tp = 1 s	5 3.5	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 150	°C °C



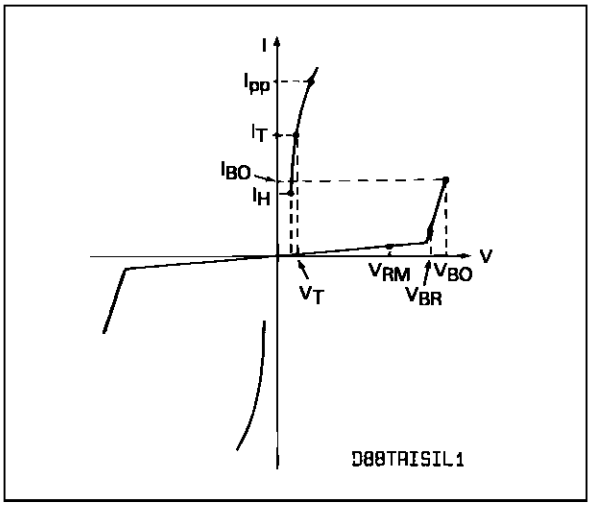
Pulse waveform 10/1000µs

THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
R_{th} (j-a)	Junction to ambient	DIL 8 SO 8	125 171	°C/W °C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
I_{BO}	Breakover current
I_{PP}	Peak pulse current
V_F	Forward Voltage Drop



Types	I_R @ V_{RM} max		VBR @ I_R min		V_{BO} max note1	VBO typ note2	I_{BO} max note1	I_H min note3	V_T max note4
	µA	V	V	mA	V	V	mA	mA	V
TPI80xxN	10	70	80	1	120	150	800	150	8
TPI120xxN	10	105	120	1	180	200	800	150	8

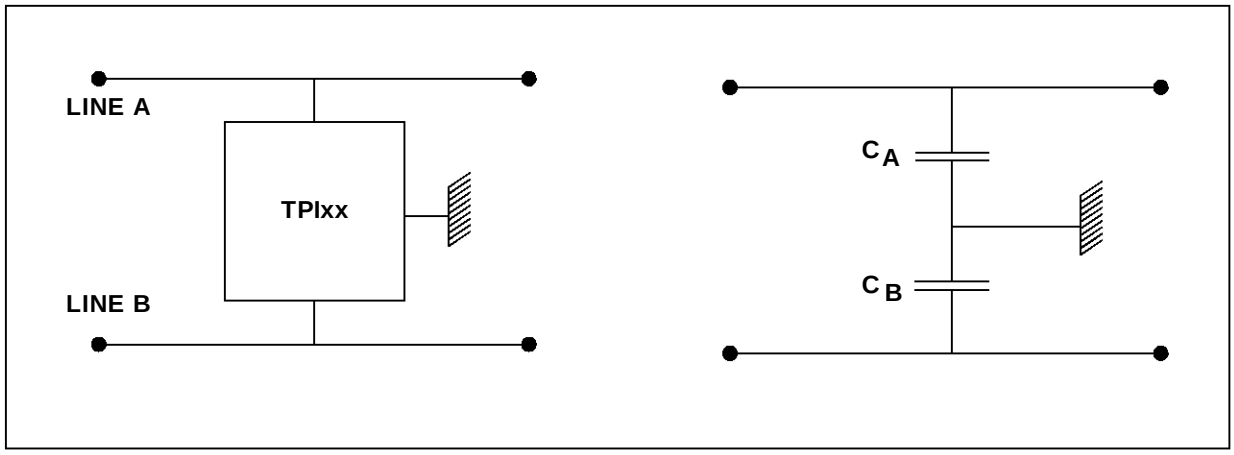
Note 1 : See the reference test circuit for I_{BO} and V_{BO} parameters.

Note 2 : Surge test according CCITT 1.5kV,10/700 µs between Tip or Ring and ground.

Note 3 : See functional holding current test circuit.

Note 4 : Square pulse Tp = 500 ms - IT = 5A.

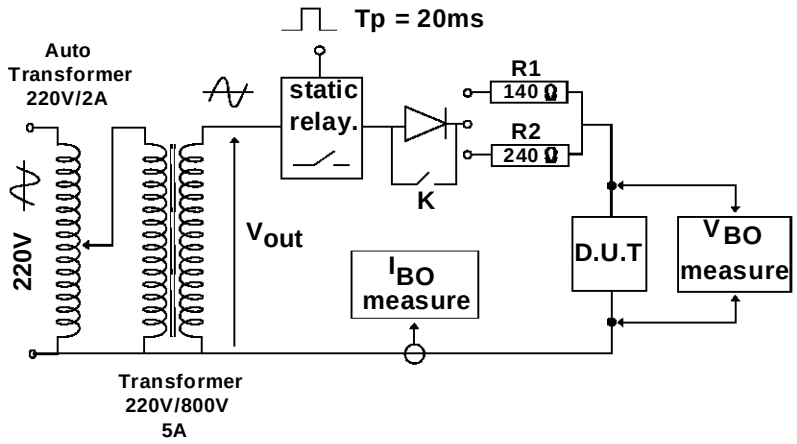
CAPACITANCES CHARACTERISTICS



CONFIGURATION	C_A (pf) max	C_B (pf) max	C_A - C_B (pf) max
V_A =1V V_B =56V	70	50	30
V_A = 56V V_B= 1V	50	70	30

All parameters tested at 25°C, except where indicated

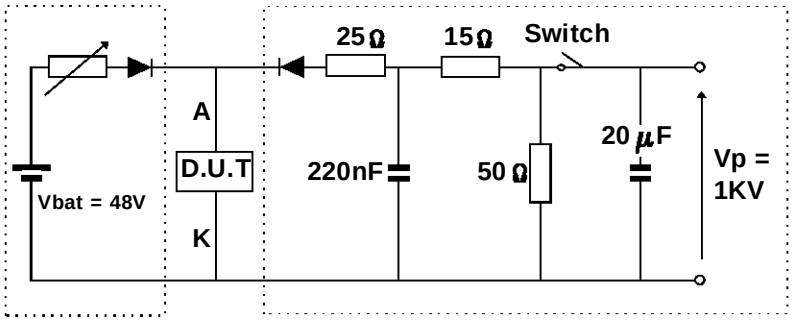
REFERENCE TEST CIRCUIT FOR I_{BO} and static V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a functional test circuit which performs a GO-NOGO test on the holding current level I_H .

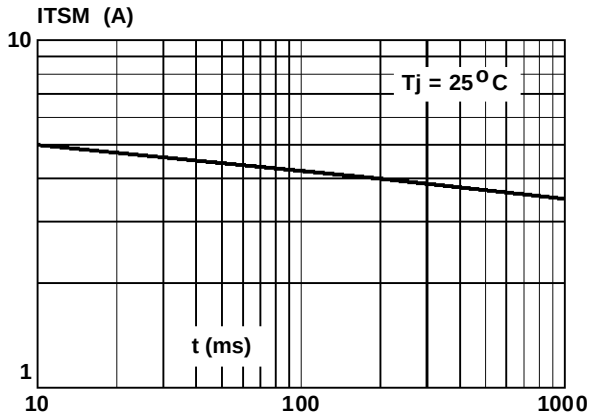
TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.

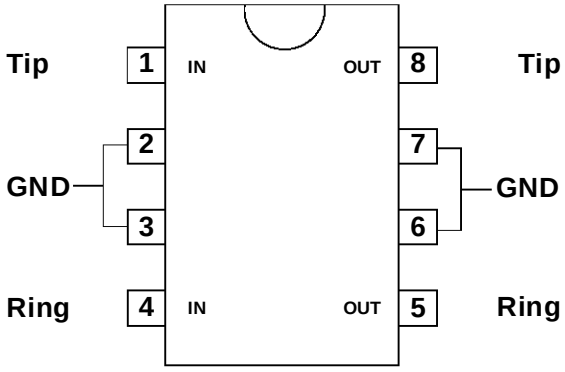
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.

3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

Fig. 1 : Non repetitive surge peak on-state current. (with sinusoidal pulse : F =50Hz)



APPLICATION NOTE.



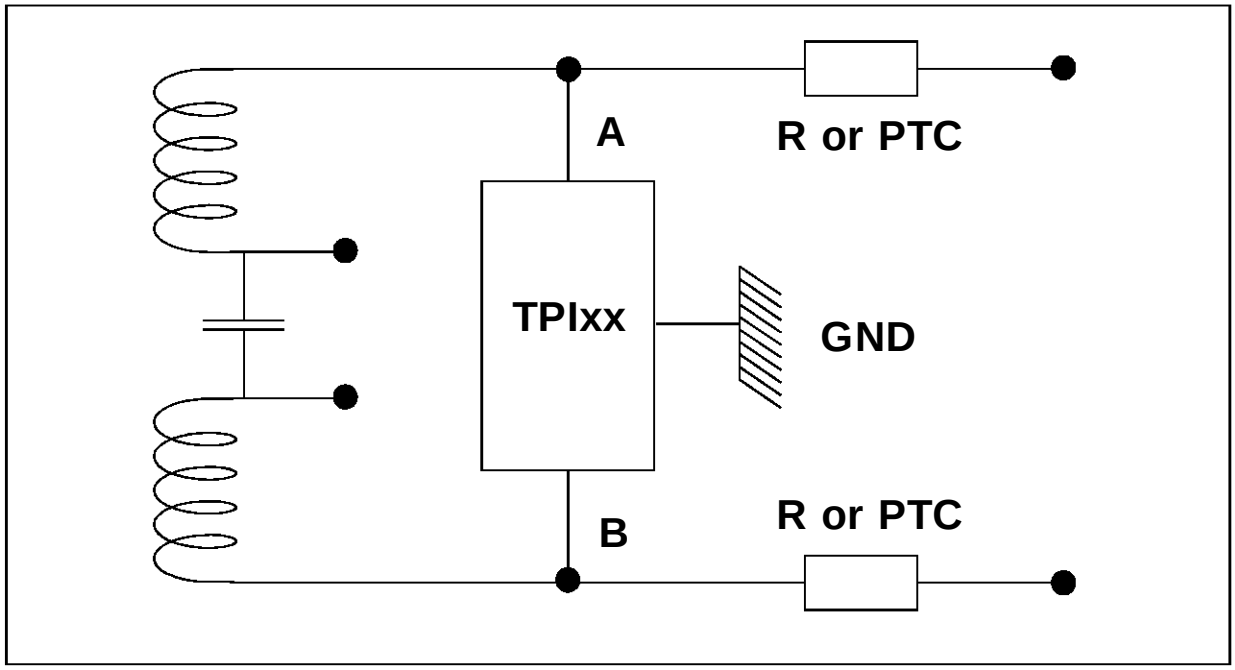
4- points structure lay-out.

1) Connect pins 2, 3, 6 and 7 to ground in order to guarantee a good surge current capability for long duration disturbances.

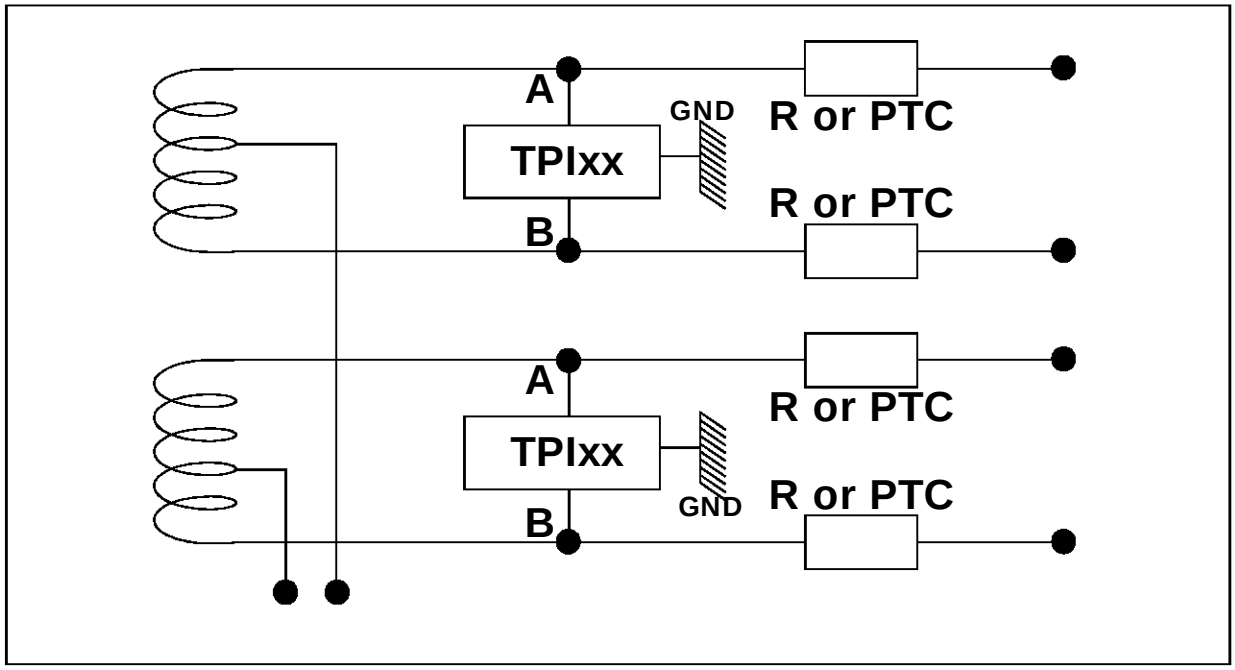
2) In order to take advantage of the "4-points structure" of the TPIxxxP, the tip and Ring lines have to cross through the device. in this case, the device will eliminate the overvoltages generated by the parasitic inductances of the wiring (Ldi/dt), especially for very fast Transients.

APPLICATION NOTE:

U INTERFACE PROTECTION

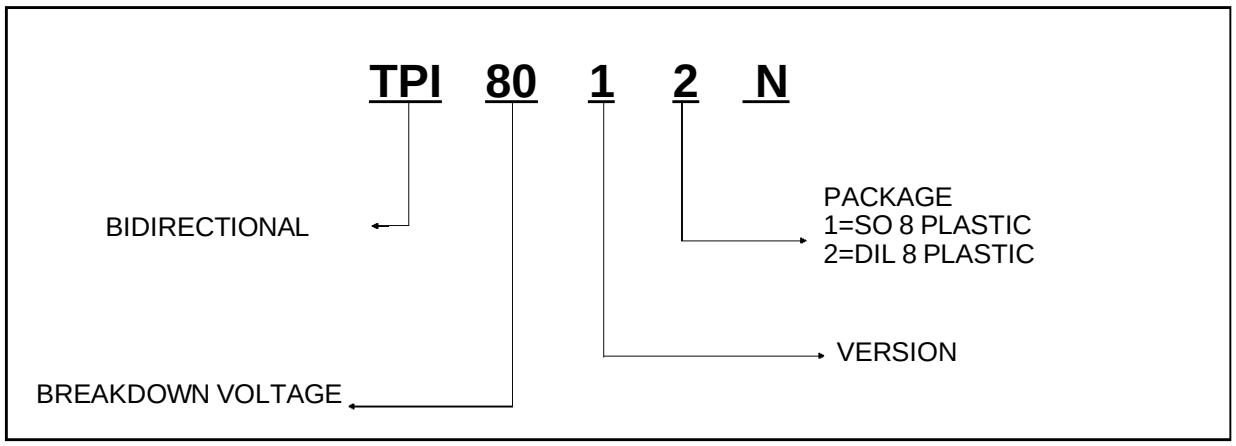


S INTERFACE PROTECTION



This component use an intemal structure resulting in symetrical characteristics with a good balanced behaviour.
This topology ensures the same breakdown voltage level for positive and negative surges in differential and common mode .

ORDER CODE



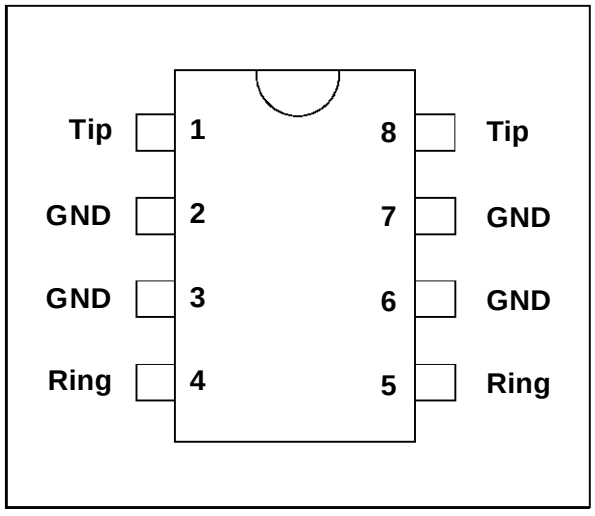
MARKING

Package	Type	Marking
SO8	TPI8011N TPI12011N	TP80N TP120N

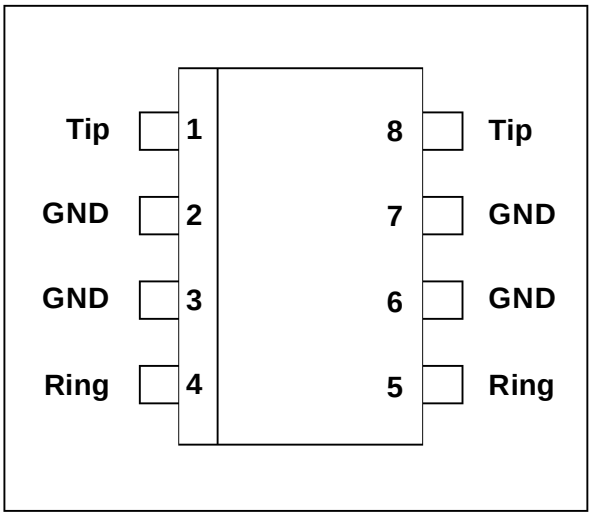
Package	Type	Marking
DIL8	TPI8012N TPI12012N	TP80N TP120N

CONNECTION DIAGRAM

DIL 8 Plastic



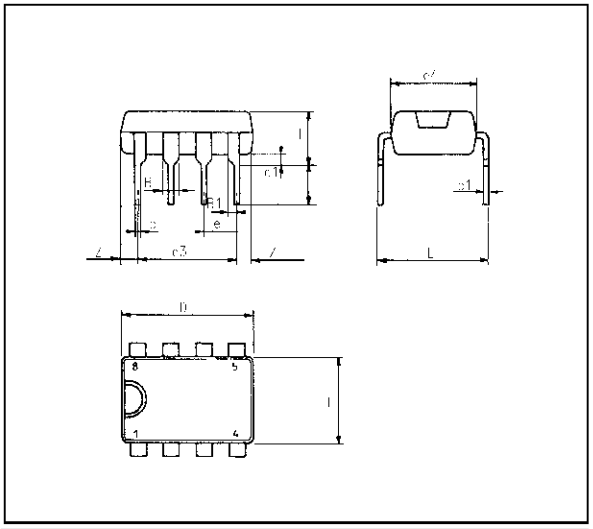
SO 8 Plastic



Packaging : Products supplied in antistatic tubes.

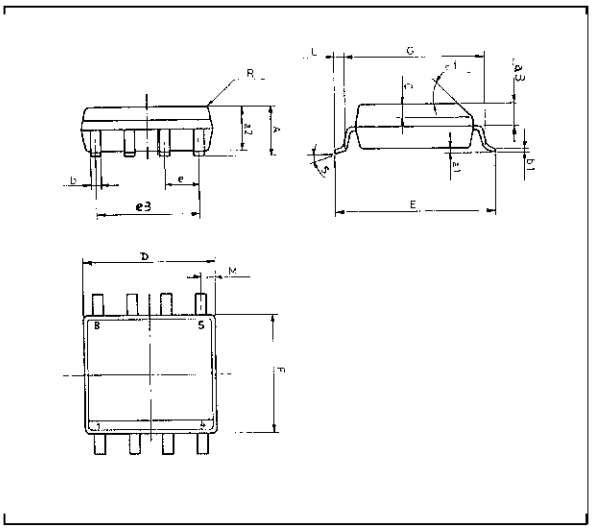
PACKAGE MECHANICAL DATA (in millimeters)

DIL 8 Plastic



REF.	DIMENSIONS					
	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.7			0.027		
B	1.39		1.65	0.054		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.50	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e4		7.52			0.300	
F			7.1			0.280
I			4.8			0.189
L	3.3			0.130		
Z	0.44		1.60	0.017		0.063

SO 8 Plastic



REF.	DIMENSIONS					
	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max)					

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